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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/411,792	10/01/1999	David Alan Eward	99-TK-238	8808

7590 11/14/2005

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EXAMINER	
VO, TED T	
ART UNIT	**PAPER NUMBER**
2191	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/411,792	EWARD ET AL.	
	Examiner	Art Unit	
	Ted T. Vo	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the RCA filed on 09/06/2005, on the Claims filed on 09/22/04.

All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b)

Claims 1-64 stand finally rejected under 35 U.S.C. 102(b) as being anticipated by Circello et al. (US No. 5,737,516).

Claims 1-64 are pending in the application.

Response to Arguments

2. Applicants' arguments in the Remarks filed on 09/06/2005 have been fully considered.

In the arguments, Applicants depict an example of "Instruction Address", where this instruction address points to an instruction memory that contains an instruction opcode and addresses of operands. Applicants contend that the instruction address, i.e. program counter value 1100100 is the address of an ADD instruction. Applicants argue that when the memory fetches the content of this memory location, it simply sees the Add instruction, and it does not see operand addresses. Applicants point out that for operands, they are stored at another memory address locations. Applicants point that the location 110010 stores the first operand and the location 111010 stores the second operand, then Applicants conclude Circello does not disclose or suggest an operand address is provided from the processor core 9 and the debug module 9 (Examiner assumes that Applicants ague for limitation: "**bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored**".

Respectfully, the depiction shown in Applicants' remarks is only one of many instruction structure seen in binary code executed by a microprocessor. In the case of the Applicants' depiction, it is only a case of **indirect address** where in many program instructions the operands might be located by address references in an instruction content. However, the question is why Applicants do not depict an ADD address in which the **operand values are directly after an opcode**, e.g. "ADD a, b", "SUB a, b", etc., where a and b are the direct operand values. When a stored address in Circello pointing to these instructions, it will be also the address of a or of b. For a typical example, "ADD a, b", the address instruction "1100100" will be address of opcode "ADD" and also the address of operand a or operand b. It should be noted that an address a house points to all members rein the house. Therefore, instruction address has the same means of opcode address, or operand address, or an indirect address of an operand, depending the fetch content of the instruction.

It also noted that, the specification (p. 4: 4-7) includes instruction address,

"wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least one of: an operand address; an instruction address, and a performance status".

Based on this specification passage, it mentions only the common structures of an instruction, such as an operand address, **an instruction address**, and a performance status. These things are known as program instructions. According to the arguments, Applicants has maintained the "operand address" to be patentable over "instruction address". However, they fail to clearly point out the patentable novelty (See MPEP 714.04, CFR 1.111(c)). Because Applicants have maintained the broad claims and the arguments aim to the feature that isn't novel in the art, the final rejection is applied.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-64 are rejected under 35 U.S.C. 102(b) as being anticipated by Circello et al. (US No. 5,737,516), submitted by applicants.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per Claim 1:

Circello teaches, "*At least one processor* (FIG. 1, figure feature core 9);

a debug circuit (FIG. 1, all circuitries connecting to figure feature core 9);

a system bus coupling the processor and debug circuit (*See* FIG. 1, S-BUS, M-BUS, or K-BUS etc. (*system bus*); and K-BUS, CPST, BUS REQUEST, BUS GRANT, STALL, BREAKPOINT CONTROL (*communication link*)); *and*

a communication link coupling the processor and debug circuit (see figure 2, all connections/bus between core 9 and the debug module 10), *wherein the processor is configured to transmit to the debug through the communication link a plurality of bit values each representing a state of an operation* (see Column 3, lines 54-59, having means for *transmit, operand address, representing a state*) *in the processor including at least an operand address that indicates a memory location at which an operand value is stored* (See column 20, lines 27-61, particularly, *take branch* , value on the CPST, *capture an instruction address Target at the conclusion of the IC cycle of an instruction fetch pipeline* (operand address; See Col. 14, lines 65-67 and Col. 15, lines 1-23).

As per Claim 2: Circello shows KCONTROLL and K-BUS that relates together in debugging, (column 4, lines 55-67), and discusses a pipeline operation that produces outputs to KADDR and KDATA of K-BUS (see column 6, lines 5-25).

As per Claim 3: In coupled with K-BUS, Circello discusses a register that stores program counter breakpoint (see column 9, lines 49-61).

As per Claim 4: Being inherent from debug mode operation (column 12, lines 35-39). Circello teaches that the counter program breakpoint defines a region in a local address space (see column 13, lines 37-50)

belonged to a data processing system (FIG. 1) might be used to trigger breakpoint function. It further provides pipelines accessibility to cause a step instruction execution (see started column 19, line 64 to column 20, line 61).

As per Claim 5: Circello teaches inherently the limitation in discussing the trigger response (see column 29, lines 24-40).

As per Claim 6: Regarding limitation, "a first instruction past a branch instruction", Circello teaches inherently the limitation in using the value, %0101 of the PST signal (see column 15, lines 46-50).

As per Claim 7: Circello teaches inherently the limitation in using the values of the PST signal (see column 15, lines 46-50) for indicating branch or return instructions, where the PST receives information from K-BUS.

As per Claim 8: Circello discloses real-time tracing that provides a unique trace function (see column 22, lines 14-16).

As per Claim 9: Circello discloses a PST that receives information from K-BUS to provide bit information to reflect an execution status of the CPU (see column 15, lines 10-2).

As per Claim 10: Circello discloses the PST that receives information from K-BUS to assert some of bit values for exception processing (see FIG. 10).

As per Claim 11: Circello discloses the mechanism in the figure 2 that is configured to transmit debug information to the debug module via K-Bus and control links connected to the core 9.

As per Claim 12: Circello discloses the PST that receives information from K-BUS to assert bit values (FIG. 10). Some of these bit values indicate executions of instructions.

As per Claim 13: Circello discloses the PST that receives information from K-BUS to assert bit values (FIG. 10). Some of these bit values indicate identifier information of executions. For example, one of bit values indicates that a branch is taken.

As per Claim 14: Circello provides debugging which is capable of performing exception/interrupt handling (FIG. 10, or column, 8, lines 35-41).

As per Claim 15: Claims limitation is inherent in bits values. For example, the signal from K_BUS causes the control 60 to generate PST and DDATA. The table in columns 22-23 describes bit values of the

DDATA, where these values are used by external development system to view the execution of instructions.

As per Claim 16: For a matching with a memory address access by the processor in response to an execution instruction is inherent in branching/jumping or exception/interrupt.

As per Claim 17: Being inherent in execution of single instruction step mode (column 11, lines55-56) or the status that indicates, 'begin execution of an instruction' (FIG. 10).

As per Claim 18: Circello discloses the PST that receives information from K-BUS to assert bit values (FIG. 10). Some of these bit values indicate identifier information of executions. For example, one of bit values indicates that a branch is taken.

As per Claim 19: Being inherent in execution of tracing function (see column 22, lines 14-25) or the status that indicates, 'begin execution of an instruction' (FIG. 10).

As per Claim 20: FIG. 1 has means of a single integrated circuit.

As per Claim 21:

Circello discloses, "*At least one processor* (FIG. 1, figure feature core 9);

a debug circuit (FIG. 1, all circuitries connecting to figure feature core 9);

a system bus coupling the processor and debug circuit (*See* FIG. 1, S-BUS, M-BUS, or K-BUS etc (*system bus*)); *and*

a communication link coupling the processor and debug circuit (*See* FIG. 1, K-BUS, CPST, BUS REQUEST, BUS GRANT, STALL, BREAKPOINT CONTROL (*communication link*), *where the processor is configured to transmit to the debug through the communication link a plurality of bit values each representing a state of an operation in the processor including at least one of: and*

an operand address that indicates a memory location at which an operand value is stored (See Col. 14, lines 65-67 and Col. 15, lines 1-23); *and an operand value* (*See* column 20, lines 27-61, particularly, *take branch*, value on the CPST, "capture an instruction address Target at the conclusion of the IC cycle of an instruction fetch pipeline": '*operand address and operand value*');

where the processor is further to configured to transmit to the debug circuit: a program counter value indicating the program counter of the processor at a writeback stage of a pipeline of the processor,

a status indicating that a computer instruction is in the writeback stage is valid computer instruction (*See,* Column 20, lines 27-62, *pipeline, instruction address of "Target". As the JMP instruction occupies the AGEX stage of the operand execution pipelines;* see column 13, lines 37-64, Program Counter Breakpoint, data signal transferred via K-Bus 25..."); *a status indicating that the computer instruction in the writeback stage is a first instruction past an execute branch instruction; a status indicating a type of executed branch instruction and process identifier information of an executed instruction* (*See* started from column 12, line 15 to column 13, line 64, teaching of address space that defines a range started with a breakpoint location; and see DDATA bit definitions, the table in columns 22-23).

As per Claims 22, 42: The claims have the claimed functionality corresponding to the functionality of Claim 1. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 1.

As per Claims 23, 43: The claims have the claimed functionality corresponding to the functionality of Claim 2. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 2.

As per Claim 24: The claim has the claimed functionality corresponding to the functionality of Claim 3. Claim is rejected in the same reasons set forth in connecting to the rejection of Claim 3.

As per Claims 25, 44: The claims have the claimed functionality corresponding to the functionality of Claim 4. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 4.

As per Claims 26, 45: The claims have the claimed functionality corresponding to the functionality of Claim 5. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 5.

As per Claims 27, 46: The claims have the claimed functionality corresponding to the functionality of Claim 6. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 6.

As per Claim 28, 47: The claims have the claimed functionality corresponding to the functionality of Claim 7. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 7.

As per Claim 29, 48: The claims have the claimed functionality corresponding to the functionality of Claim 8. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 8.

As per Claims 30, 49: The claims have the claimed functionality corresponding to the functionality of Claim 9. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 9.

As per Claims 31, 50: The claims have the claimed functionality corresponding to the functionality of Claim 10. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 10.

As per Claims 32, 51: The claims have the claimed functionality corresponding to the functionality of Claim 11. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 11.

As per Claims 33, 52: The claims have the claimed functionality corresponding to the functionality of Claim 12. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 12.

As per Claims 34, 53: The claims have the claimed functionality corresponding to the functionality of Claim 13. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 13.

As per Claims 35, 54: The claims have the claimed functionality corresponding to the functionality of Claim 14. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 14.

As per Claims 36, 55: The claims have the claimed functionality corresponding to the functionality of Claim 15. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 15.

As per Claims 37, 56: The claims have the claimed functionality corresponding to the functionality of Claim 16. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 16.

As per Claims 38, 57: The claims have the claimed functionality corresponding to the functionality of Claim 17. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 17.

As per Claims 39, 58: The claims have the claimed functionality corresponding to the functionality of Claim 18. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 18.

As per Claims 40, 59: The claims have the claimed functionality corresponding to the functionality of Claim 19. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 19.

As per Claims 41, 60: The claims have the claimed functionality corresponding to the functionality of Claim 20. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 20.

As per Claim 61: Circello discloses the claim limitation (See column 20, lines 27-61, particularly, *take branch*, value on the CPST, *capture an instruction address Target at the conclusion of the IC cycle of an instruction fetch pipeline* (operand address and operand value); and see FIG.2, the K-BUS connected to the to the FIFO 70; and see Col. 14, lines 65-67 and Col. 15, lines 1-23).

As per Claim 62: Circello discloses the claim limitation (See column 20, lines 27-61, particularly, *take branch*, value on the CPST, *capture an instruction address Target at the conclusion of the IC cycle of an instruction fetch pipeline* (operand address and operand value); and see FIG.2, the K-BUS connected to the to the FIFO 70, and see Col. 14, lines 65-67 and Col. 15, lines 1-23);

As per Claims 63, 64: The claims have the claimed functionality corresponding to the functionality of Claim 62. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 62.

Conclusion

5. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 5:30PM.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Freescale Semiconductor, "Motorola Version Three ColdFire® Processor – Advanced Processors for the Next Generation of Storage, Imaging, and Multimedia Products", White paper, www.freescale.com, pages: 1-15, 1997.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708.

The facsimile number for the organization where this application or proceeding is assigned is the Central Facsimile number **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted T. Vo
Primary Examiner
Art Unit 2191
November 10, 2005